ECC has developed a helical interleaving technique that increases the burst error correction capability of TPCs. The burst error correction capabilities of the resulting TPCs is quite dramatic. In this note, we provide some simulation results to quantify this for the (4096,3249) TPC as well as the (4096,1311) TPC.

At the encoder, helical interleaving defines the order in which bits from an encoded block of data are read out to the modulator. At the receiver, helical deinterleaving defines the order in which bits from the demodulator are read into the decoder. Figure 1 illustrates the helical interleaving process for the two dimensional (4096,3249) TPC. The first bit (labeled bit 0) to be read out of the encoder is in the upper left-hand corner of the array. The second bit is from the second row, second column, the third bit is from the third row third column and so on diagonally until the lower right hand corner is reached. Then, the 65th bit is the first row in the second column. This process continues until the last bit (the 4096th bit) is read from the array. Thus, when the last row is reached, wrap around to the first unread row. Similarly, when the last column is reached wrap around to the first unread column. Helical interleaving in the three dimensional codes follows the same logic except that instead of reading diagonally through an array of data, we read diagonally through a cube of data.

![Helical Interleaving of the (4096,3249) TPC](image)

**Figure 1 : Helical Interleaving of the (4096,3249) TPC**
Mathematically, helical interleaving for the 2-Dimensional TPCs can be computed as follows. If the original elements in a 2-D array were indexed via rows and columns (such as in an array in software or a RAM in hardware), the index for helically reading the bits is computed as

\[
j = i (n_x + 1) \mod (n_x n_y) \quad i = \{0, 1, 2, \ldots, n_x n_y - 1\}
\]

where \(i\) is the original index, \(j\) is the helical index, \(n_x\) is the number of bits in the x dimension code and \(n_y\) is the number of bits in the y dimension code. Similarly, in the 3-D case the helical index is computed as

\[
j = i (n_x n_y + n_x + 1) \mod (n_x n_y n_z) \quad i = \{0, 1, 2, \ldots, n_x n_y n_z - 1\}
\]

where \(n_z\) is the z dimension code. In both cases, helical interleaving is implemented as an addressing scheme that requires very little additional complexity.

To assess the performance benefits of helical interleaving, we simulated the performance of the (4096,3249) TPC and the (4096,1311) TPC with various length burst error events. A burst error event of length \(L\) is defined as a string of encoded bits whose amplitude levels are set equal to zero. AWGN is then added to the transmitted sequence as usual. Figure 2 illustrates the performance associated with burst error events of 128, 256, and 384 bits for the (4096,3249) TPC. Figure 3 illustrates the performance associated with burst error events of 128, 384, 640, and 1024 (25% of the block) bits for the (4096,1311) TPC. Three effects on the performance can be seen. First, as expected, the Eb/No required to obtain a given BER increases as the burst length increases. However, as shown in Table 2, even with bursts that are large percentages of the total block, the TPC can still close the link. Second, as the burst length increases the slope of the BER curves decreases, thus requiring more incremental SNR to achieve the same reduction in BER. The third observation is that when bursts of increasing longer lengths are presented, the BER curve will start to flare. This is expected, since at some point when the burst event is longer than the code can correct, increasing the SNR won’t reduce the error rate causing the BER curve to flatten at some BER rate.

<table>
<thead>
<tr>
<th>Code Parameters</th>
<th>Burst Length L (# of bits)</th>
<th>% of Total Block</th>
<th>Degradation at BER=10^-6 (dB)</th>
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</thead>
<tbody>
<tr>
<td>(4096,3249) TPC</td>
<td>128</td>
<td>3.125</td>
<td>1.3</td>
</tr>
<tr>
<td>(4096,3249) TPC</td>
<td>256</td>
<td>6.250</td>
<td>3.8</td>
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<tr>
<td>(4096,3249) TPC</td>
<td>384</td>
<td>9.375</td>
<td>6.25</td>
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<td>(4096,1311) TPC</td>
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<tr>
<td>(4096,1311) TPC</td>
<td>1024</td>
<td>25.000</td>
<td>4.8</td>
</tr>
</tbody>
</table>
Figure 2: Helically Interleaved (4096,3249) TPC Burst Error Performance
Figure 3: Helically Interleaved (4096,1311) TPC Burst Error Performance

(4096,1331) TPC Burst Error Performance
(63 Axis Iterations = 21 Full Iterations)

Information Eb/No (dB)

Bit Error Rate (BER)

- No Burst Errors
- Burst Event = 128 Bits
- Burst Event = 384 Bits
- Burst Event = 640 Bits
- Burst Event = 1024 Bits